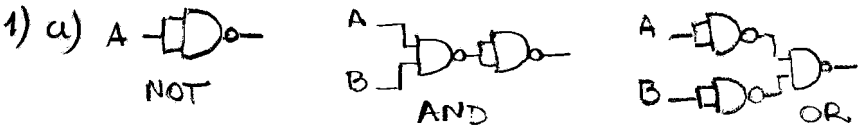
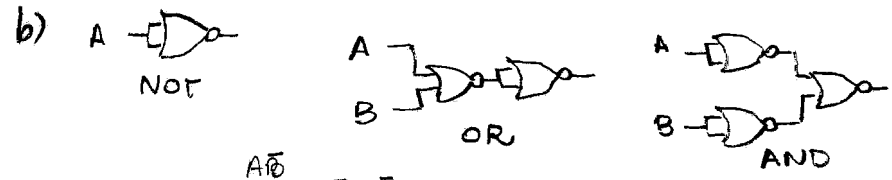
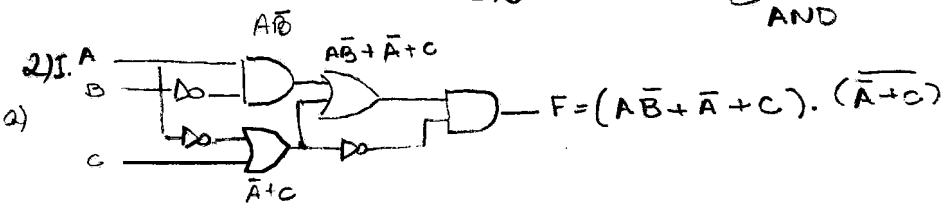
lista circuitos digitais (3)

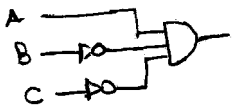
1) a) 

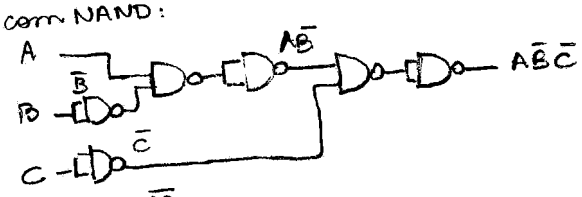
b) 

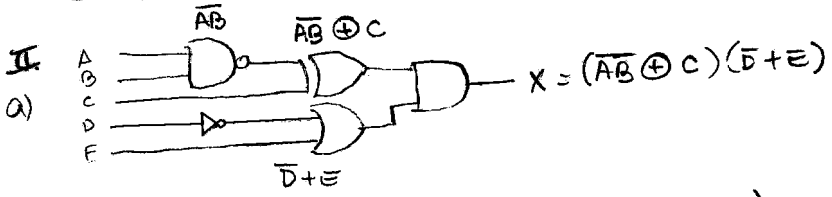
2) I. a) 

b) $(A\bar{B}+A+C)(\overline{\bar{A}+C}) = (A\bar{B}+\bar{A}+C)(A\bar{C})$

$(\bar{A}+\bar{B}+C)(A\bar{C}) = (\cancel{\bar{A}A} + A\bar{B} + AC)\bar{C} = A\bar{B}\bar{C} + \cancel{AC\bar{C}} = A\bar{B}\bar{C}$

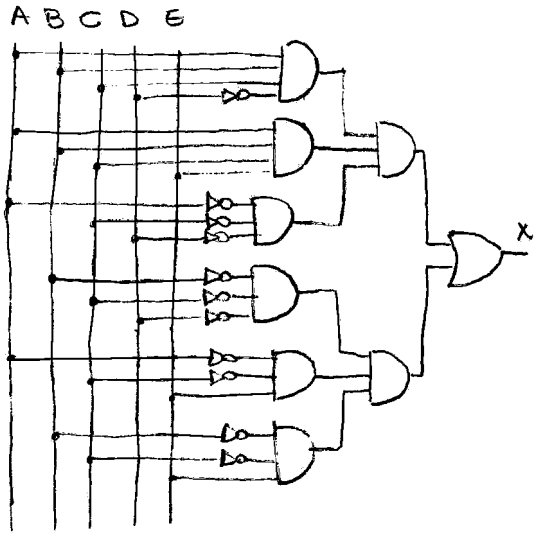


c) com NAND: 

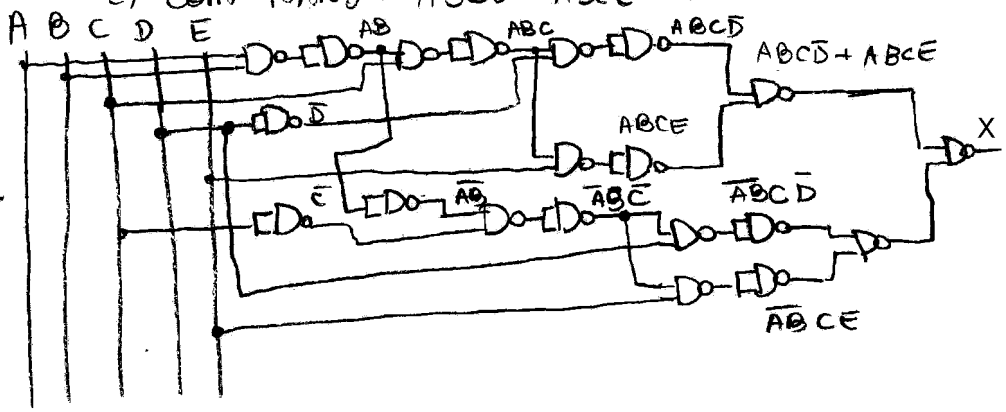
II. a) 

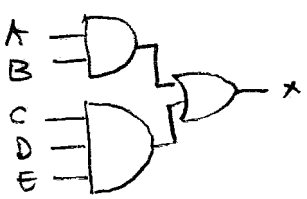
b) $(\overline{AB}\oplus C)(\bar{D}+E) = (\overline{\overline{AB}C} + \overline{AB}\bar{C})(\bar{D}+E) = ABC\bar{D} + ABCE + (\bar{A}+\bar{B})\bar{C}\bar{D} + (\bar{A}+\bar{B})\bar{C}E$

$ABC\bar{D} + ABCE + \bar{A}\bar{C}\bar{D} + \bar{B}\bar{C}\bar{D} + \bar{A}\bar{C}E + \bar{B}\bar{C}E$



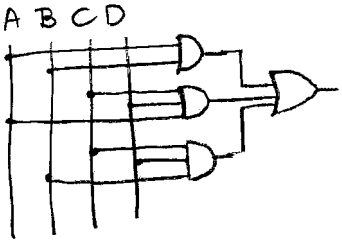
c) com NAND: $ABC\bar{D} + ABCE + \overline{A\bar{B}}\,\bar{C}D + \overline{A\bar{B}}\bar{C}E$

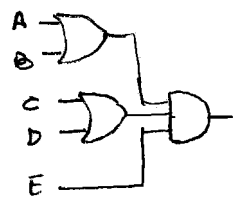


3) a) 

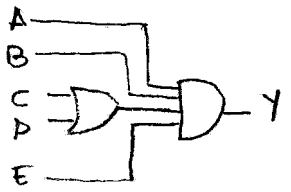
b) $AB + CD(A+B)$

$AB + CDA + CDB$

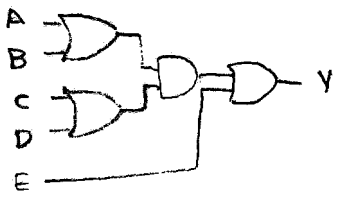


c) 

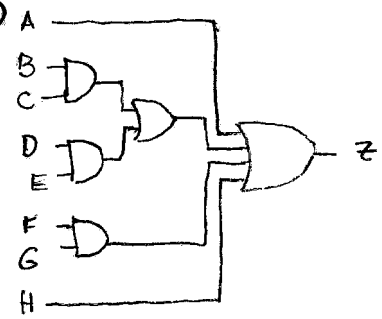
d)



e)

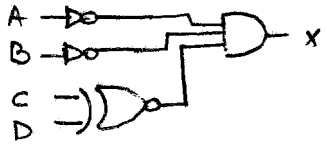


f)

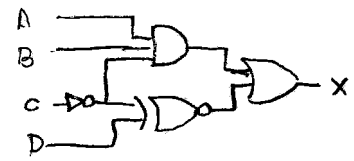


g)

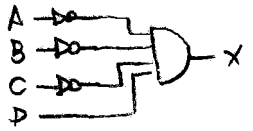
h)



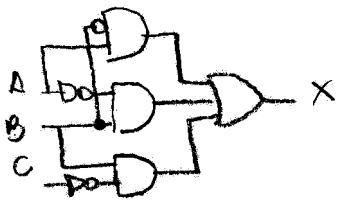
i)



j) $\bar{A}\bar{B}\bar{C}D$



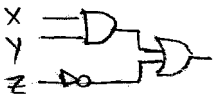
k)



4 a)

	$\bar{Y}\bar{Z}$	$\bar{Y}Z$	YZ	$Y\bar{Z}$
$\bar{X}$	1	0	0	1
X	1	0	1	1

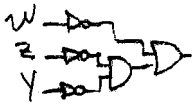
$XY + \bar{Z}$



b)

	$\bar{Z}\bar{W}$	$\bar{Z}W$	ZW	$Z\bar{W}$
$\bar{X}\bar{Y}$	1	1	0	1
$\bar{X}Y$	1	0	0	1
XY	1	0	0	1
$X\bar{Y}$	1	1	0	1

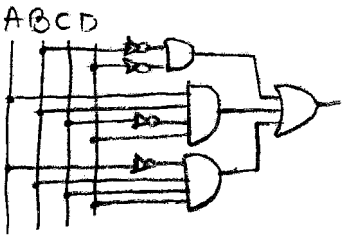
$\bar{W} + \bar{Z}\bar{Y}$



c)

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	0	1
$\bar{A}B$	0	0	1	0
AB	0	1	0	0
$A\bar{B}$	1	0	0	1

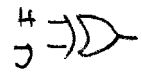
$\bar{B}\bar{D} + AB\bar{C}D + \bar{A}BCD$



d)

	$\bar{I}\bar{J}$	$\bar{I}J$	IJ	$I\bar{J}$
$\bar{G}\bar{H}$	0	1	1	0
$\bar{G}H$	1	0	0	1
GH	1	0	0	1
$G\bar{H}$	0	1	1	0

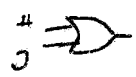
$H\bar{J} + J\bar{H} = H \oplus J$



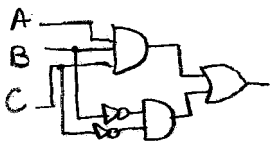
e)

	$\bar{I}\bar{J}$	$\bar{I}J$	IJ	$I\bar{J}$
$\bar{G}\bar{H}$	0	1	1	0
$\bar{G}H$	1	1	1	1
GH	1	1	1	1
$G\bar{H}$	0	1	1	0

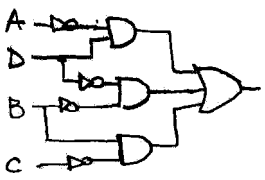
$H + J$



5) a) $\bar{C}\bar{B} + ABC$



b) $\bar{B}\bar{D} + \bar{A}D + B\bar{C}$



6)

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	0	0
$\bar{A}B$	0	0	1	0
AB	1	1	1	1
$A\bar{B}$	0	0	1	0

3b- $A + (B + CD)(A + B)$

$A + AB + B + ACD + BCD$

$CD(A + B) + A(1 + B) + B$

$AB + B + CD(A + B)$

$B(A + 1) + CD(A + B)$

$AB + ACD + BCD$

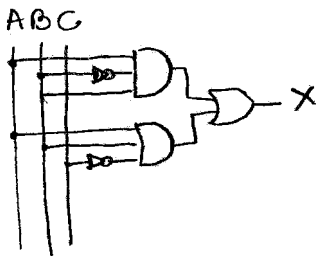
(vide circuito 3b)

3g) $X = A(B \oplus C)$

$= A(\bar{B}C + B\bar{C})$

$= A\bar{B}C + AB\bar{C}$

$\bar{C}$ \ $\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}$	0	(1)	0
C	0	0	(1)



3h) $X = (\overline{A+B})(C \oplus (A+\bar{D}))$

$(\bar{A}\bar{B})[\bar{C}(A+\bar{D}) + C\overline{(A+\bar{D})}]$

$(\bar{A}\bar{B})[\bar{C}A + \bar{C}D + C(\bar{A}D)]$

$\bar{A}\bar{B}(\bar{C}A + \bar{C}D + C\bar{A}D)$

~~$\bar{A}\bar{B}\bar{C}A$~~ $+ \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}CD$

$\bar{A}\bar{B}(\bar{C}\bar{D} + CD) = \bar{A}\bar{B}(\overline{C \oplus D})$

(vide circuito 3h)

forma mínima: $\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD$

$\bar{A}\bar{B}$ \ $\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	(1)	0	(1)	0
$\bar{A}B$	0	0	0	0
AB	0	0	0	0
$A\bar{B}$	0	0	0	0

3i) $X = B\bar{C}A + \overline{(\bar{C} \oplus D)}$

$= B\bar{C}A + \overline{(\bar{\bar{C}}D + \bar{C}\bar{D})}$

$= B\bar{C}A + \overline{(CD + \bar{C}\bar{D})}$

$= B\bar{C}A + (\bar{C} + \bar{D})(C + D)$

$= B\bar{C}A + (\bar{C}C + \bar{C}D + \bar{D}C + \bar{D}\bar{D})$

$= AB\bar{C} + (C \oplus D)$ → vide circuito 3i)

$= AB\bar{C} + \bar{C}D + C\bar{D}$

$\bar{A}\bar{B}$ \ $\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	0	1
$\bar{A}B$		1		1
AB	1	1	0	1
$A\bar{B}$	0	1	0	1

3j) $X = ((A + \overline{B \oplus D})(\bar{C} \to A) + B)\overline{A + B}$

$= ((A + \overline{\bar{\bar{B}}D + \bar{B}\bar{D}})(\bar{C} + A) + B)\bar{A}\bar{B}$

$= (((A + (\bar{B} + \bar{D})(B + D))(\bar{C} + A) + B)\bar{A}\bar{B}$

$= ((A + \bar{B}B + \bar{B}D + \bar{D}B + \bar{D}\bar{D})(\bar{C} + A) + B)\bar{A}\bar{B}$

$= (A\bar{C} + A\bar{A} + \bar{B}D\bar{C} + \bar{B}DA + \bar{D}B\bar{C} + \bar{D}BA + B)\bar{A}\bar{B}$

$= (A\bar{C} + \bar{B}\bar{C}D + A\bar{B}D + B\bar{C}\bar{D} + AB\bar{D})\bar{A}\bar{B}$

$= (A\bar{A}C + \bar{A}\bar{B}\bar{C}D + A\bar{A}\bar{B}D + \bar{A}B\bar{C}\bar{D} + AB\bar{D})\bar{B}$

$= \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{B}\bar{C}\bar{D} + AB\bar{B}\bar{D}$

$= \bar{A}\bar{B}\bar{C}D$ (vide circuito 3j)

$\bar{A}\bar{B}$ \ $\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	(1)	0	0
$\bar{A}B$	0	0	0	0
AB	0	0	0	0
$A\bar{B}$	0	0	0	0

3k) $X = A \oplus B + \bar{C}B + \bar{A}$

$= \bar{A}B + A\bar{B} + \bar{C}B + \bar{A}$

$= \bar{A}B + A\bar{B} + \bar{C}B$

$\bar{C}$ \ $\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}$	0	(1 1)	1	(1)
C	0	(1)	0	(1)

vide circuito 3k

7) Circuito montado com logisim

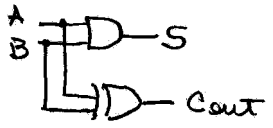
8) Somador ripple carry de n bits

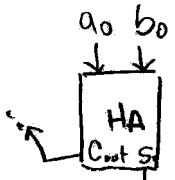
- Sem carry in: meio somador (HA)

a_0	b_0	S_0	C_{out}
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Saída S_0: $A \oplus B$

$C_{out} = AB$





1 porta AND de 2 entradas

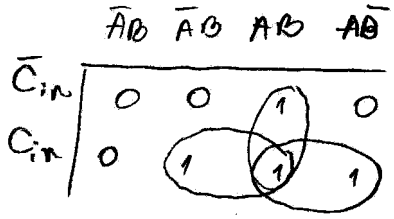
1 porta XOR de 2 entradas

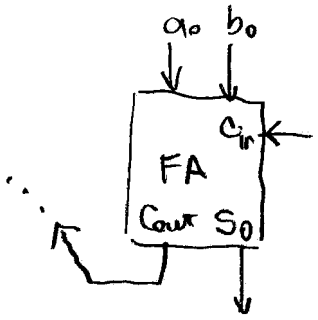
- Com carry in: somador completo (FA)

C_{in}	a_0	b_0	S_0	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = A \oplus B \oplus C$

$C_{out} = AB + BC + AC$

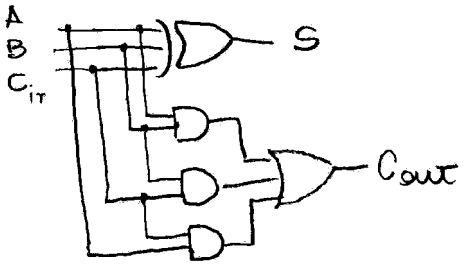




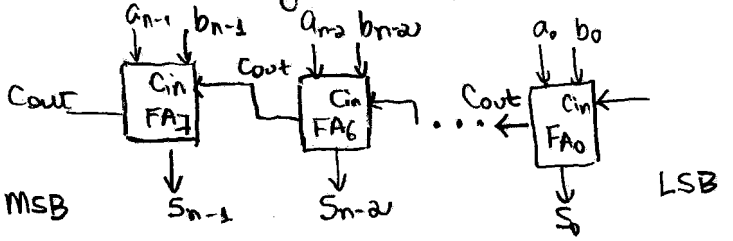
3 portas AND de 2 entradas

1 porta XOR de 3 entradas

1 porta OR de 3 entradas



9) 8 somadores completos de 4 bits em cascata (carry in do somador i recebe carry out do somador $i-1$, $0 < i \leq n-1$)

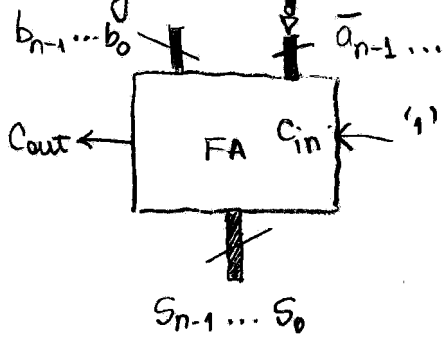


10) Subtrator completo de n bits:

Lembrar que a subtração pode ser feita com complemento de 2:

$$B - A = B + \bar{A} + 1$$

Colocar carry in = 1 para o LSB



↳ invertidos com portas NOT.

11) Feito no logisim

12) Palavra $X = x_{n-1} x_{n-2} \dots x_1 x_0$ em complemento de 2

$F_2 := /x < 0$ $\quad F_2 = x_{n-1}$

$F_1 := /x = 0$ $\quad F_1 = \overline{x_{n-1}} \; \overline{(x_{n-2} + x_{n-3} + \dots + x_0)}$

$F_0 := /x > 0$ $\quad F_0 = \overline{x_{n-1}} \; (x_{n-2} + x_{n-3} + \dots + x_0)$

Ideia: MSB (x_{n-1}) define o sinal da palavra:

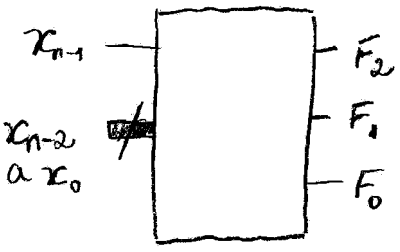
$x_{n-1} = 1$ é negativo $\begin{cases} F_2 = 1 \\ F_1 = 0 \\ F_0 = 0 \end{cases}$

$x_{n-1} = 0$ é não negativo $F_2 = 0$

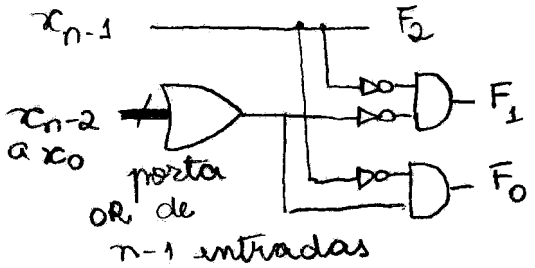
Para decidir se é positivo ou zero:

$x_{n-1} = 0$ e <u>todos</u> os demais bits $(x_{n-2}, \dots, x_0) = 0$ é zero $\begin{cases} F_2 = 0 \\ F_1 = 1 \\ F_0 = 0 \end{cases}$

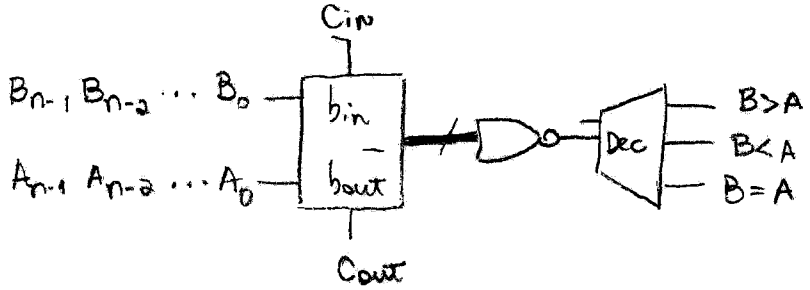
$x_{n-1} = 0$ e <u>pelo menos</u> um bit $(x_{n-2}, \dots, x_0) = 1$ é positivo $\begin{cases} F_2 = 0 \\ F_1 = 0 \\ F_0 = 1 \end{cases}$



Circuito interno



13)



14) Overflow (V) para números sem sinal: carry out = 1

V para números com sinal em complemento de 2:

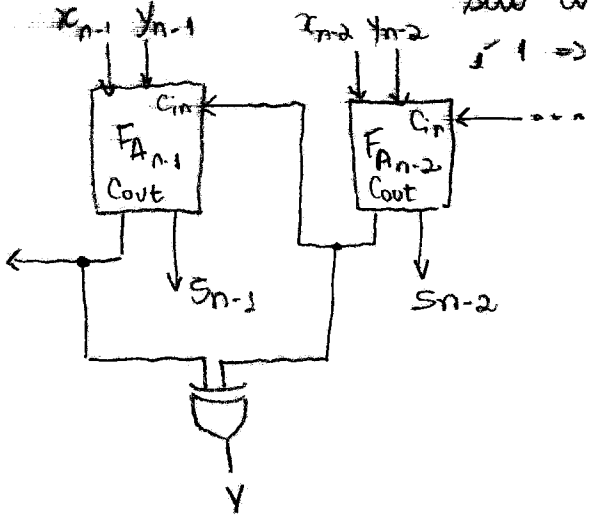
- se os números tem sinais opostos, nunca ocorre overflow
- se os números tem o mesmo sinal e o MSB da soma tem sinal diferente, ocorreu overflow.

Uma maneira mais simples: observar carry in e carry out do MSB:

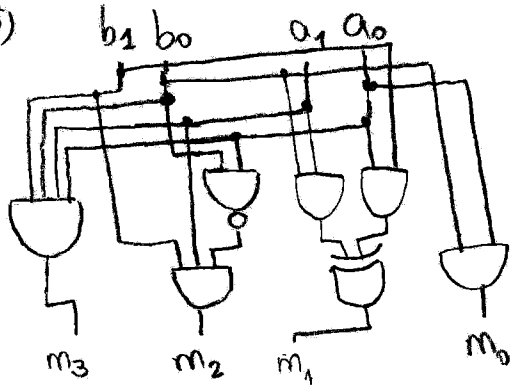
Cin	Cout	V
0	0	0
0	1	1
1	0	1
1	1	0

- quando carry in = 0 e ocorre carry out = 1 significa que x_{n-1} e y_{n-1} são ambos negativos (1) e MSB da soma é 0 ⇒ overflow
- quando carry in = 1 e ocorre carry out = 0 significa que x_{n-1} e y_{n-1} são ambos positivos (0) e MSB da soma é 1 ⇒ overflow.

$C_{in} \oplus C_{out}$



15)



16) Entradas: $n+1$

$(x_{n-1}, x_{n-2}, \dots x_0, y)$

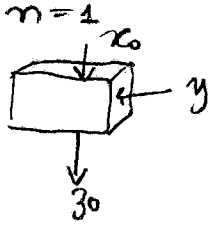
saídas: n

$(z_{n-1}, z_{n-2}, \dots z_0)$

$z_i \begin{cases} 0 \text{ se } y=0 \\ x_i \text{ se } y=1 \end{cases}$

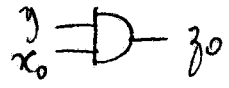
$\forall i,\ 0 \le i \le n-1$

para $n=1$

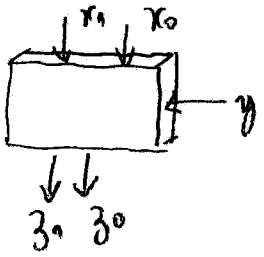


y	x_0	z_0
0	0	0
0	1	0
1	0	0
1	1	1

$z_0 = y \cdot x_0$



para $n=2$

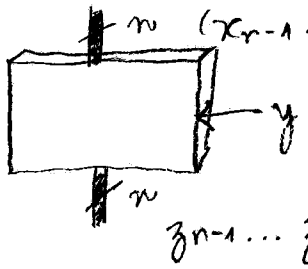


y	x_1	x_0	z_1	z_0
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

$z_1 = y x_1 \bar{x}_0 + y x_1 x_0 = y x_1$

$z_2 = y \bar{x}_1 x_0 + y x_1 x_0 = y x_0$

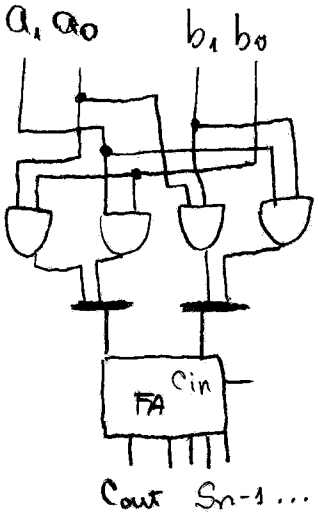
Seletor de $n+1$ entradas:



$z_i = y \cdot x_i$

$\forall i,\ 0 \le i \le n-1$

17)



Para n bits

$a_{n-1}\ a_{n-2} \dots a_1\ a_0$

$b_{n-1}\ b_{n-2} \dots b_1\ b_0$

$2n$ produtos canônicos de entrada no somador completo

18) Codificador 2 para 1

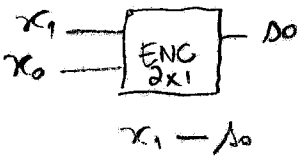
entradas ativas nível alto

entradas ativas nível baixo

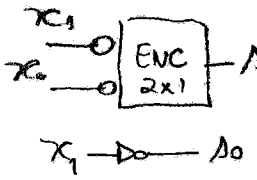
2x1:

x_0	x_1	s_0
0	1	0
1	0	1

$s_0 = x_1$



$x_1 - s_0$



$x_1 - s_0$

demais entradas da Tabela resultam em don't care

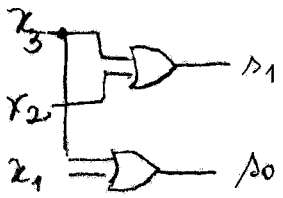
4x2

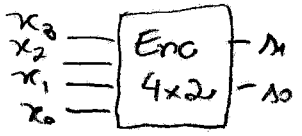
x_3	x_2	x_1	x_0	s_1	s_0
0	0	0	1	0	0
0	0	1	0	0	(1)
0	1	0	0	(1)	0
1	0	0	0	(1)	(1)

$s_1 = x_2 + x_3$

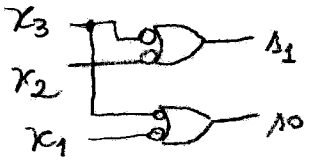
$s_0 = x_1 + x_3$

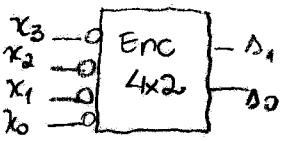
Entradas em nível alto





entradas em nível baixo





8x2.

x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0	s_0	s_1	s_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	(1)
0	0	0	0	0	1	0	0	0	(1)	0
0	0	0	0	1	0	0	0	0	(1)	(1)
0	0	0	1	0	0	0	0	(1)	0	0
0	0	1	0	0	0	0	0	(1)	0	(1)
0	1	0	0	0	0	0	0	(1)	(1)	0
1	0	0	0	0	0	0	0	(1)	(1)	(1)

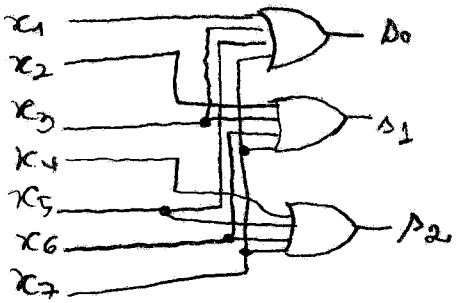
Para entradas em nível baixo, haverá apenas uma entrada ativa em 0, as demais entradas ficam em 1

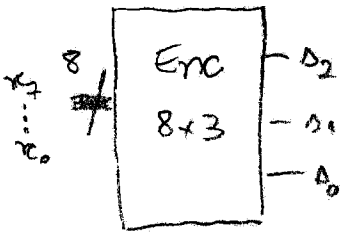
$s_2 = x_4 + x_5 + x_6 + x_7$

$s_1 = x_2 + x_3 + x_6 + x_7$

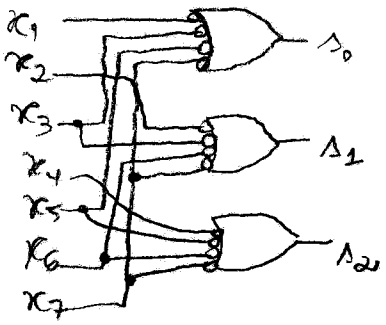
$s_0 = x_1 + x_3 + x_5 + x_7$

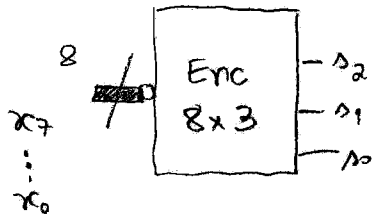
entradas em nível alto



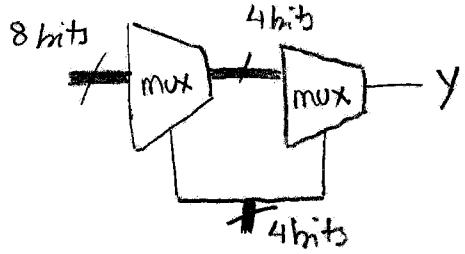


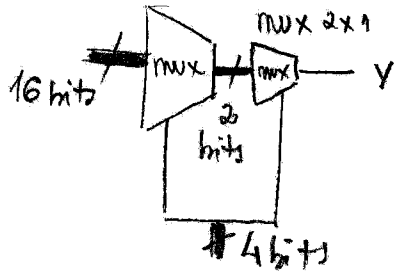
entradas em nível baixo





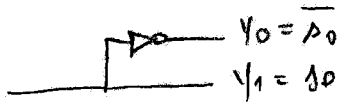
19) a) mux 16x1 com mux 4x1: b) mux 16x2 com mux 2x1:



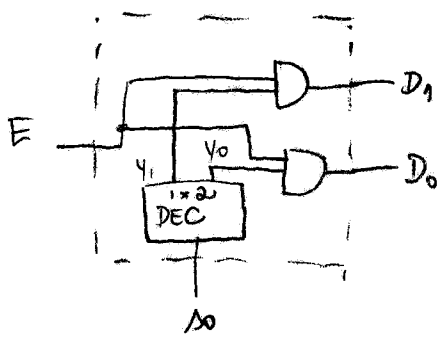


20) a) Demux usando decodificadores:

entrada	saídas	
S_0	y_1	y_0
0	0	1
1	1	0



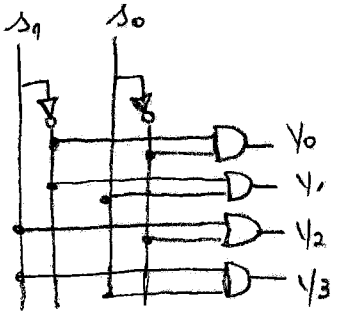
Demux 1x2



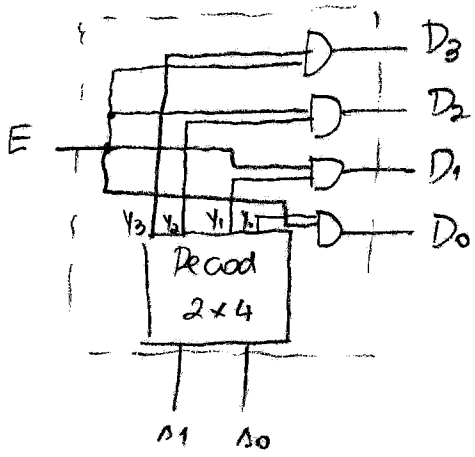
b) 1x4 Demux usando decoder 2x4

S_1	S_0	y_3	y_2	y_1	y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

$y_0 = \overline{S_1}\,\overline{S_0}$
$y_1 = \overline{S_1}\,S_0$
$y_2 = S_1\,\overline{S_0}$
$y_3 = S_1\,S_0$
(minitermos)



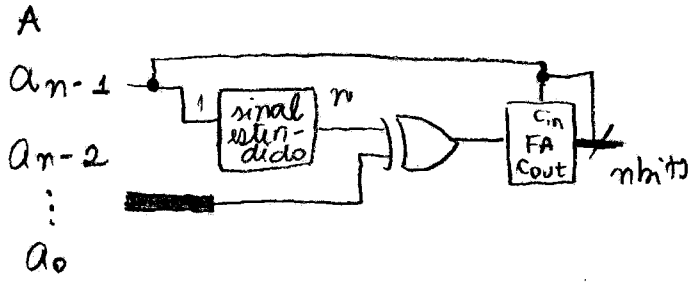
Demux 1x4



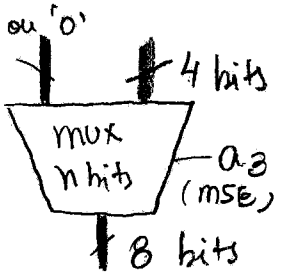
c) 1x8 Demux usando Decoder 3x8 ⇒ 8 saídas do decoder ($y_7 \dots y_0$) AND E fornecem saídas do Demux $D_7 \dots D_0$

d) 1x16 Demux usando Decoder 4x16 ⇒ 16 saídas do decoder ($y_{15} \dots y_0$) AND E fornecem saídas do Demux $D_{15} \dots D_0$

21)

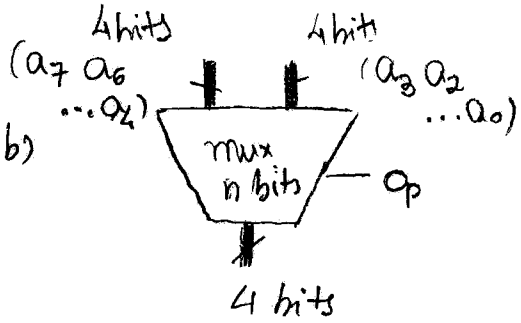


22) a)



Solução: verificar o sinal de A (a_3 é op)
se for 1, acrescenta 4 '1' à esquerda do MSB de A
se for 0, acrescenta 4 '0' à esquerda do MSB de A

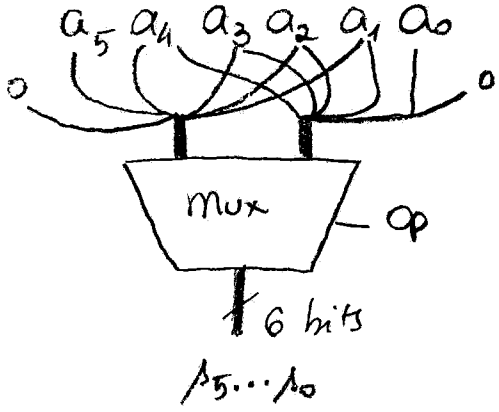
b)



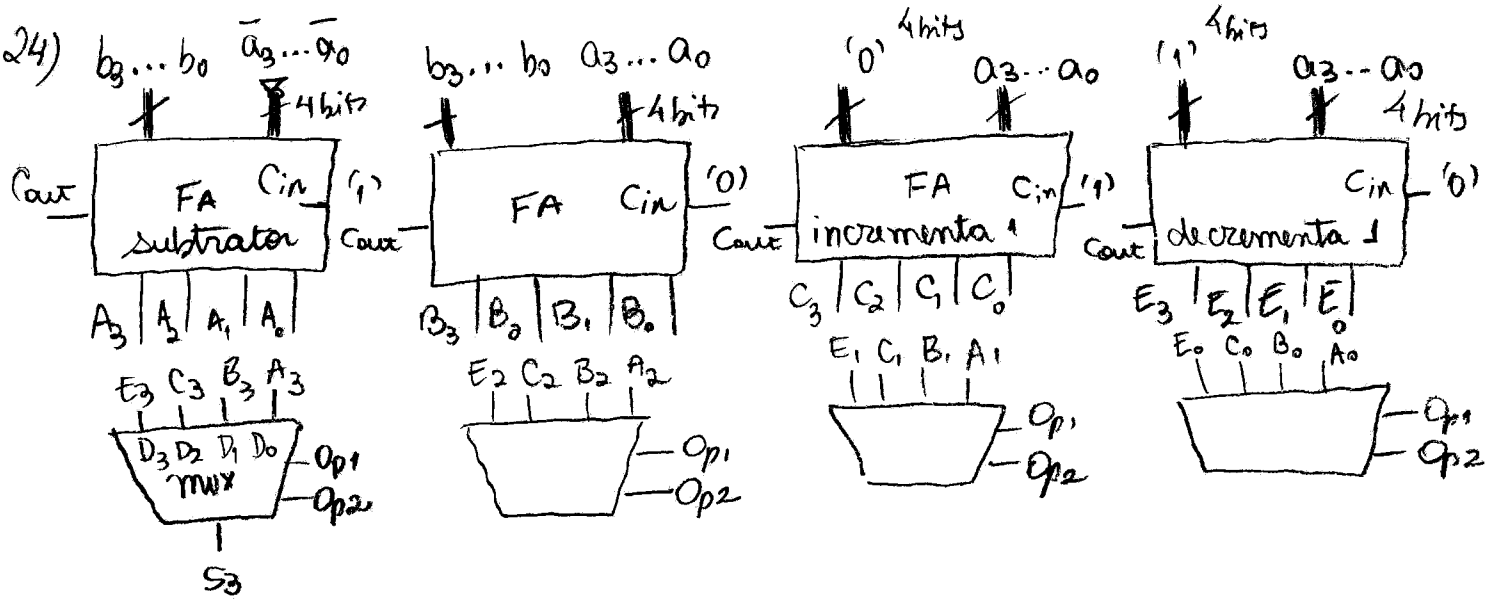
Solução: descartar os 4 dígitos LSB de A

Generalizando, basta utilizar n bits em a) e 2n bits em b)

23)



24)



25) Se somarmos ou subtrairmos números com sinais contrários nunca ocorrerá overflow ou underflow. Isto porque operandos com sinais contrários nunca podem ser maiores do que qualquer dos operandos. O overflow ocorre quando somamos dois operandos positivos e obtemos um resultado negativo, e vice-versa